

Application No.: 10/671,273

Docket No.: JCLA9302

AMENDMENTS**In The Specification:**

Please amend paragraph [0032] as follows:

[0032] One source/drain terminal (or the first source/drain terminal of the third PMOS transistor) of the PMOS transistor 406 (or the third PMOS transistor) is electrically connected to the capacitor 440 and the substrate (or the substrate of the third PMOS transistor) of the PMOS transistor 406. The other source/drain terminal (or the second source/drain terminal of the third PMOS transistor) of the PMOS transistor 406 is electrically connected to the voltage source for receiving an input voltage V_{IN} . Similarly, one source/drain terminal (or the first source/drain terminal of the fourth PMOS transistor) of the PMOS transistor 408 (or the fourth PMOS transistor) is electrically connected to the capacitor ~~[[430]]~~440 and the substrate (or the substrate of the fourth PMOS transistor) of the PMOS transistor 408. The other source/drain terminal (or the second source/drain terminal of the fourth PMOS transistor) of the PMOS transistor 408 is electrically connected to the gate (or the gate of the third PMOS transistor) of the PMOS transistor 406. Furthermore, the gate (or the gate of the fourth transistor) of the PMOS transistor 408 is electrically connected to the voltage source for receiving the input voltage V_{IN} .

Please amend paragraph [0036] as follows:

[0036] Conversely, because the clocking signal CK is at 0V, the NMOS transistor 418 is non-conductive. Since the gate terminal of the NMOS transistor 416 receives the input voltage V_{IN} , the NMOS transistor 416 conducts and hence the voltage value at the source/drain terminal of the NMOS transistor 416, the source/drain terminal of the PMOS transistor 406 and the gate of the PMOS transistor 406 approach V_{IN} . Since the voltage value at the gate terminal of the

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PMOS transistor 408 is V_{IN} , which is at a high level causing the PMOS transistor 408 ~~[[is]]~~ to be non-conductive. Similarly, because the input voltage V_{IN} received by the source/drain terminal of the PMOS transistor 406 is close to the voltage received by the gate terminal, the PMOS transistor ~~[[402]]~~406 is non-conductive. Therefore, the second output voltage from the output terminal V_{OUT2} is roughly identical to the inverted clocking signal CK' . In other words, the second output voltage from the output terminal V_{OUT2} approaches V_{IN} .

Please amend paragraph [0038] as follows:

[0038] Thereafter, as the clocking signal CK reverses, the PMOS transistor 402 and 404 will be conductive~~[[again]]~~. Thus, voltage at the output terminal V_{OUT1} is maintained at V_{IN} . On the other hand, because the PMOS transistors 406 and 408 are non-conductive, voltage at the output terminal V_{OUT2} is maintained at V_{IN} . Under the condition that the capacitor 440 ~~[[terminal 440b]]~~ receives a voltage V_{IN} from the inverted clocking signal CK' , the second output voltage from the output terminal V_{OUT2} is $2 \cdot V_{IN}$.

Please amend paragraph [0042] as follows:

[0042] In addition, one source/drain terminal (or the first source/drain terminal of the seventh PMOS transistor) of the PMOS transistor 566 (or the seventh PMOS transistor) is electrically connected to the second output terminal V_{OUT2} . The other source/drain terminal (or the second source/drain terminal of the seventh PMOS transistor) of the PMOS transistor 566 is electrically connected to a final output terminal 590 for outputting a final output voltage V_O . The substrate (or the substrate of the seventh PMOS transistor) of the PMOS transistor 566 is electrically connected to the substrate and source/drain terminal of the PMOS transistor 562.

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The gate (or the gate of the seventh PMOS transistor) of the PMOS transistor 566 is electrically connected to the ~~[[second]]~~first output voltage terminal ~~[[V_{OUT2}]]~~ V_{OUT1}. One source/drain terminal (or the first source/drain terminal of the eighth PMOS transistor) of the PMOS transistor 568 (or the eighth PMOS transistor) is electrically connected to the first output voltage terminal V_{OUT1}. The other source/drain terminal (or the second source/drain terminal of the eighth PMOS transistor) of the PMOS transistor 586 is electrically connected to the final output terminal 590. The substrate (or the substrate of the eighth PMOS transistor) of the PMOS transistor 568 is electrically connected to the substrate of the PMOS transistor 564. The gate (or the gate of the eighth PMOS transistor) of the PMOS transistor 568 is electrically connected to the ~~[[first]]~~second output voltage terminal ~~[[V_{OUT1}]]~~ V_{OUT2}.